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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/843,823	04/30/2001	Meng-Chang Yang	YANG3002/EM/6747	9945

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EXAMINER	
HANNETT, JAMES M	
ART UNIT	**PAPER NUMBER**
2612	

DATE MAILED: 04/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/843,823	YANG ET AL.	
	Examiner	Art Unit	
	James M Hannett	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 4-8* is/are rejected.

7)☒ Claim(s) *1 and 4-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 10/29/2004 have been fully considered but they are not persuasive.

The applicant argues that new claim 6 recites perpendicularly arranged wires, rather than vertically arranged wires. The examiner points out that the perpendicular electrodes 2 and 3 depicted in Figure 16 of Izumi et al are also vertically relative to each other so that they can overlap at point (4) and not touch each other. Therefore, the examiner views the electrodes (2 and 3) as depicted in Figure 16 as being perpendicularly arranged and vertically arranged.

The applicant argues that the prior art does not teach the use of two voltage sources that are both separate and different as claimed. The examiner asserts that although the two different voltages may be derived from the save original voltage source, the examiner views any circuit that generates two distinct voltages as having two different voltage sources. The two different voltage sources, is viewed by the examiner as the two distinct circuit arrangements that generate the two distinct voltages (Vres and Vdd) in Wayne.

Claim Objections

Claims 1, 4-8 are objected to because of the following informalities: The applicant inadvertently duplicated the limitation "a reset transistor connected to the first source" in claims 1 and 6. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1: Claims 1, and 4-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 6,753,912 Wayne in view of USPN 6,618,083 Chen et al in further view of USPN 6,437,341 Izumi et al.

2: As for Claim 1, Wayne teaches on Column 3, Lines 31-65 and depicts in Figure 1 and 2 An active pixel sensor comprising: a first voltage source (Vref) and a second voltage source (Vdd); a reset transistor (T5) connected to the first voltage source (Vref); a photoelectric element (PD) connected to the reset transistor (T5) for being charged by the first voltage source (Vref) when the reset transistor (T5) is turned on; and a source follower transistor (T2), a readout switch transistor (T1), and a bias transistor (T3) connected in series and supplied with power from the second voltage source (Vdd), the source follower transistor (T2) having a gate connected to a connection point between the reset transistor (T6) and the photoelectric element (PD), the bias transistor (T3) establishing a predetermined bias for the source follower transistor (T2), so as to read out a photoelectric signal from the connecting point when the readout switch transistor (T1) is turned on. Wayne teaches that two voltages are used Vref and Vdd. However, Wayne does not specifically state that he two voltages sources have different voltage levels.

Chen et al teaches on Column 3, Lines 60 - Column 4, Line 25 and depicts in Figure 1 a CMOS pixel with the same configuration of Wayne et al. Chen et al teaches these of two voltage sources Vres and Vdd. Chen et al teaches that it is advantageous to set Vres and Vdd to be different in order to suppress the mismatch effect caused by a non-ideal reset switch.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to set Vref less than Vdd as taught by Chen et al in the image sensor of Wayne in order to suppress the mismatch effect caused by a non-ideal reset switch.

Wayne in view of Chen et al teaches the use of a pixel circuit that outputs image data to a CDS circuit. Wayne in view of Chen et al teaches that the pixel circuit is supplied with two voltage signals (Vref) and (Vdd). However, Wayne in view of Chen et al is silent as to the layout of the individual circuit elements on the image sensor chip and is further silent as to the wiring of the metal wires used to supply the desired voltage signals to the correct circuit elements.

Izumi et al teaches on Column 16, Lines 26-46 and depicts in Figure 16 that it is advantageous when manufacturing integrated circuits that require a plurality of metal wires, to supply the wires on different layers of vertically arranged metal wires, thereby eliminating noise interference caused by parasitic capacitance of the metal wires and saving layout space.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to supply the wires for (Vref and Vdd) of Wayne in view of Chen et al on different layers of vertically arranged metal wires as taught by Izumi et al, thereby eliminating noise interference caused by parasitic capacitance of the metal wires and saving layout space.

3: In regards to Claim 4, Chen et al further teaches on Column 4, Lines 2-15 the first and second voltage sources are adjusted when the active pixel sensor is operating. Chen et al teaches that the voltage values of (Vres and Vdd) will be changed depending on the operating condition (for example a wide temperature range, bright-light sensing, and dark sensing).

4: As for Claim 5, Wayne further teaches on Column 3, Lines 57-65 and depicts in Figure 1 the pixel sensor has an output end connected to a correlated double sampling circuit.

5: In regards to Claim 6, Wayne teaches on Column 3, Lines 31-65 and depicts in Figure 1 and 2 An active pixel sensor comprising: a first voltage source (Vref) and a second voltage source (Vdd); a reset transistor (T5) connected to the first voltage source (Vref); a photoelectric element (PD) connected to the reset transistor (T5) for being charged by the first voltage source (Vref) when the reset transistor (T5) is turned on; and a source follower transistor (T2), a readout switch transistor (T1), and a bias transistor (T3) connected in series and supplied with power from the second voltage source (Vdd), the source follower transistor (T2) having a gate connected to a connection point between the reset transistor (T6) and the photoelectric element (PD), the bias transistor (T3) establishing a predetermined bias for the source follower transistor (T2), so as to read out a photoelectric signal from the connecting point when the readout switch transistor (T1) is turned on. Wayne teaches that two voltages are used Vref and Vdd. However, Wayne does not specifically state that he two voltages sources have different voltage levels.

Chen et al teaches on Column 3, Lines 60 - Column 4, Line 25 and depicts in Figure 1 a CMOS pixel with the same configuration of Wayne et al. Chen et al teaches these of two voltage sources Vres and Vdd. Chen et al teaches that it is advantageous to set Vres and Vdd to be different in order to suppress the mismatch effect caused by a non-ideal reset switch.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to set Vref less than Vdd as taught by Chen et al in the image sensor of Wayne in order to suppress the mismatch effect caused by a non-ideal reset switch.

Wayne in view of Chen et al teaches the use of a pixel circuit that outputs image data to a CDS circuit. Wayne in view of Chen et al teaches that the pixel circuit is supplied with two voltage signals (Vref) and (Vdd). However, Wayne in view of Chen et al is silent as to the layout

of the individual circuit elements on the image sensor chip and is further silent as to the wiring of the metal wires used to supply the desired voltage signals to the correct circuit elements.

Izumi et al teaches on Column 16, Lines 26-46 and depicts in Figure 16 that it is advantageous when manufacturing integrated circuits that require a plurality of metal wires, to supply the wires on different layers of vertically arranged metal wires that are perpendicularly oriented to each other. This is depicted in Figure 16 by electrodes 3 and 2, thereby eliminating noise interference caused by parasitic capacitance of the metal wires and saving layout space.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to supply the wires for (Vref and Vdd) of Wayne in view of Chen et al on different layers of vertically arranged metal wires that are perpendicular as taught by Izumi et al, thereby eliminating noise interference caused by parasitic capacitance of the metal wires and saving layout space.

6: As for Claim 7, Claim 7 is rejected for reasons discussed related to Claim 4.

7: In regards to Claim 8, Claim 8 is rejected for reasons discussed related to Claim 5.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M Hannett whose telephone number is 571-272-7309. The examiner can normally be reached on 8:00 am to 5:00 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on 571-272-7308. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James M. Hannett
Examiner
Art Unit 2612

JMH
April 6, 2005